

THAT WHICH IS CLAIMED IS:

1. A semiconductor-on-insulator field effect transistor, comprising:
an electrically insulating layer;
5 an unstrained silicon active layer on said electrically insulating layer;
an insulated gate electrode on a surface of said unstrained silicon active layer;
and
a $\text{Si}_{1-x}\text{Ge}_x$ layer disposed between said electrically insulating layer and said
unstrained silicon active layer, said $\text{Si}_{1-x}\text{Ge}_x$ layer forming a first junction with said
10 unstrained silicon active layer and having a graded concentration of Ge therein that
decreases monotonically in a first direction extending from a peak level towards the
surface.
2. The transistor of Claim 1, wherein the peak level is greater than
15 $x=0.15$; and wherein the concentration of Ge in said $\text{Si}_{1-x}\text{Ge}_x$ layer varies from the
peak level to a level less than about $x=0.1$ at the first junction.
3. The transistor of Claim 2, wherein the concentration of Ge in said $\text{Si}_{1-x}\text{Ge}_x$
layer varies from the peak level where $0.2 < x < 0.4$ to a level where $x=0$ at the first
20 junction.
4. A semiconductor-on-insulator field effect transistor, comprising:
an electrically insulating layer;
a composite semiconductor active region on said electrically insulating layer,
25 said composite semiconductor active region comprising an unstrained silicon active
layer having a thickness greater than about $600\text{\AA}$ and a single $\text{Si}_{1-x}\text{Ge}_x$ layer disposed
between said electrically insulating layer and said silicon active layer, said $\text{Si}_{1-x}\text{Ge}_x$
layer forming a first junction with said silicon active layer and having a graded
concentration of Ge therein that decreases monotonically in a first direction extending
30 from a peak level towards a surface of said silicon active layer; and
an insulated gate electrode on the surface.

5. The transistor of Claim 4, wherein the peak level is greater than $x=0.15$; and wherein the concentration of Ge in said $\text{Si}_{1-x}\text{Ge}_x$ layer varies from the peak level to a level less than about $x=0.1$ at the first junction.

5 6. The transistor of Claim 5, wherein the concentration of Ge in said $\text{Si}_{1-x}\text{Ge}_x$ layer varies from the peak level where $0.2 < x < 0.4$ to a level where $x=0$ at the first junction.

7. A PMOS field effect transistor, comprising:
10 a composite semiconductor active region on said electrically insulating layer, said composite semiconductor active region comprising a single $\text{Si}_{1-x}\text{Ge}_x$ layer having a graded concentration of Ge therein that decreases monotonically in a first direction extending from a peak level within the single $\text{Si}_{1-x}\text{Ge}_x$ layer towards a surface thereof and a silicon active layer that extends from a first junction with the single $\text{Si}_{1-x}\text{Ge}_x$
15 layer to the surface, said composite semiconductor active region having a retrograded N-type dopant profile therein with a minimum level adjacent the surface and a peak level in the single $\text{Si}_{1-x}\text{Ge}_x$ layer; and
an insulated gate electrode on the surface.

20 8. The transistor of Claim 7, wherein the silicon active layer has a thickness greater than about $600\text{\AA}$ and has an unstrained region therein adjacent the surface.

9. The transistor of Claim 8, further comprising:
25 lightly doped P-type source and drain regions that extend in the silicon active layer and opposite the insulated gate electrode; and
a source-side pocket implant region of N-type conductivity that extends between said lightly doped P-type source region and the single $\text{Si}_{1-x}\text{Ge}_x$ layer and forms rectifying and nonrectifying junctions therewith, respectively.

30 10. An enhancement-mode field effect transistor, comprising:
an electrically insulating layer;
a silicon active layer on said electrically insulating layer;
an insulated gate electrode on a surface of said silicon active layer;

a $\text{Si}_{1-x}\text{Ge}_x$ epitaxial layer disposed between said electrically insulating layer and said silicon active layer, said $\text{Si}_{1-x}\text{Ge}_x$ epitaxial layer forming a first junction with said silicon active layer;

lightly doped source and drain regions of first conductivity type in said silicon active layer; and

a source-side pocket implant region of second conductivity type that extends between said lightly doped source region and said $\text{Si}_{1-x}\text{Ge}_x$ epitaxial layer and forms rectifying and non-rectifying junctions therewith.

10 11. The transistor of Claim 10, wherein said $\text{Si}_{1-x}\text{Ge}_x$ epitaxial layer has a graded concentration of Ge therein that decreases in a direction from said electrically insulating layer to said insulated gate electrode.

15 12. The transistor of Claim 11, wherein said $\text{Si}_{1-x}\text{Ge}_x$ epitaxial layer has a retrograded N-type dopant profile therein.

13. The transistor of Claim 12, wherein said silicon active layer has a thickness greater than about $600\text{\AA}$.

20 14. A semiconductor-on-insulator substrate, comprising:
a silicon wafer having an electrically insulating layer thereon;
a $\text{Si}_{1-x}\text{Ge}_x$ layer having a graded concentration of Ge therein extending on the electrically insulating layer; and
an unstrained silicon active layer extending on and forming a non-rectifying
25 junction with the $\text{Si}_{1-x}\text{Ge}_x$ layer and extending to a surface of the semiconductor-on-insulator substrate.

15. The substrate of Claim 14, wherein said $\text{Si}_{1-x}\text{Ge}_x$ layer is epitaxially grown from said unstrained silicon active layer.

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16. The substrate of Claim 15, wherein said unstrained silicon active layer has a thickness greater than about $600\text{\AA}$.

17. A method of forming a field effect transistor, comprising the steps of:

forming an insulated gate electrode on a surface of a semiconductor-on-insulator substrate that comprises an electrically insulating layer, an unstrained silicon active layer on the electrically insulating layer and a $\text{Si}_{1-x}\text{Ge}_x$ epitaxial layer having a graded concentration of Ge therein disposed between the electrically insulating layer and the unstrained silicon active layer;

forming source and drain regions of first conductivity type in the unstrained silicon active layer; and

forming source-side and drain-side pocket implant regions of second conductivity type that extend in the unstrained silicon active layer and in the $\text{Si}_{1-x}\text{Ge}_x$ epitaxial layer and form respective P-N junctions with the source and drain regions.

18. The method of Claim 17, wherein the unstrained silicon active layer has a thickness greater than about $600\text{\AA}$.

19. A semiconductor-on-insulator field effect transistor, comprising:
a bulk silicon region;

an electrically insulating layer on said bulk silicon region;

an unstrained silicon active layer having a first thickness on said electrically insulating layer;

an insulated gate electrode on a surface of said unstrained silicon active layer;
sidewall insulating spacers on said insulated gate electrode;

a $\text{Si}_{1-x}\text{Ge}_x$ layer of first conductivity type disposed between said electrically insulating layer and said unstrained silicon active layer, said $\text{Si}_{1-x}\text{Ge}_x$ layer forming a first junction with said unstrained silicon active layer and having a graded concentration of Ge therein that decreases monotonically in a first direction extending from a peak level towards the surface;

lightly doped source and drain regions of second conductivity type extending in said unstrained silicon active layer and having a thickness less than the first thickness; and

a source-side pocket implant region of first conductivity type in said unstrained silicon active layer, said source-side pocket implant region extending between said lightly doped source region and said $\text{Si}_{1-x}\text{Ge}_x$ layer.